The Invention Claimed Is:

1. Dynamic phase alignment circuitry comprising:

a source of a plurality of phase-distributed clock signals; and

circuitry for selecting two, phase-adjacent ones of the clock signals that currently have transitions on respective opposite sides of transitions in a serial data signal, the circuitry separately monitoring the consistency with which each of the selected two, phase-adjacent clock signals has transitions on each side of the transitions in the serial data signal and further selecting one of the selected two clock signals based on the consistency.

2. The circuitry defined in claim 1 further comprising:

output circuitry for outputting the further selected one clock signal for use as a basis for selecting sampling times of the serial data signal to recover data therefrom.

3. The circuitry defined in claim 2 wherein the circuitry for selecting makes no change in its clock signal selections unless a consistency measure threshold is reached for one of the selected two clock signals.

4. The circuitry defined in claim 3 wherein the circuitry for selecting employs different consistency measure thresholds for each of the selected two clock signals.

5. The circuitry defined in claim 4 wherein the circuitry for selecting employs a greater consistency measure threshold for the further selected one clock signal than for the other of the selected two clock signals.

6. The circuitry defined in claim 5 wherein as long as the circuitry for detecting detects that the transitions in the selected two clock signals are predominantly on respective opposite sides of the transitions in the serial data signal, the circuitry for detecting makes no change in its clock signal selections unless the consistency measure threshold for the further selected one clock signal is reached before the consistency measure threshold for the other of the selected two clock signals is reached.

7. The circuitry defined in claim 6 wherein as long as the circuitry for detecting detects that the transitions in the selected two clock signals are predominantly on respective opposite sides of the transitions in the serial data signal, the circuitry for detecting outputs a lock signal when the consistency measure threshold for the other of the selected two clock signals is reached before the consistency measure threshold for the further selected one clock signal is reached.

8. A method for dynamic phase alignment comprising:

selecting two phase-adjacent ones of a plurality of phase-distributed clock signals;

comparing phases of the selected two phase-adjacent clock signals to phase of a serial data signal; and

changing the selected phase-adjacent clock signals until the phases of the selected two phase-adjacent clock signals are predominantly on respective opposite sides of the phase of the serial data signal, and thereafter changing the selected phase-adjacent clock signals only if a first of those signals becomes more predominantly on one side of the phase of the serial data signal than a second of those signals by a predetermined amount.

9. The method defined in claim 8 further comprising:

selecting the first of the selected phase-adjacent clock signals as a basis for controlling timing of sampling of the serial data signal to recover data therefrom.

10. The method defined in claim 8 wherein the comparing comprises:

producing a first or second indication each time the phase of the first selected clock signal is on a first or second side of the phase of the serial data signal, respectively; and

producing a third or fourth indication each time the phase of the second selected clock signal is on a first or second side of the phase of the serial data signal, respectively.

11. The method defined in claim 10 wherein the comparing further comprises:

maintaining a first net count of the first and second indications; and

maintaining a second net count of the third and fourth indications.

12. The method defined in claim 11 wherein the comparing further comprises:

producing a fifth or sixth indication whenever the first net count equals a first threshold due to more first indications than second indications or vice versa, respectively; and

producing a seventh or eighth indication whenever the second net count equals a second threshold due to more third indications than fourth indications or vice versa, respectively.

13. The method defined in claim 12 wherein the first and second thresholds have different values.

14. The method defined in claim 13 further comprising:

selecting the first selected clock signal as a basis for controlling timing of sampling of the serial data signal to recover data therefrom.

15. The method defined in claim 14 wherein the first threshold is greater than the second threshold.

16. The method defined in claim 15 wherein the changing comprises:

responding to any of the fifth through eighth indications by then examining the net count that did not cause the fifth through eighth indication.

17. The method defined in claim 16 wherein the changing further comprises:

making a determination of whether and how to change at least one of the selected phase-adjacent clock signals based on whether the fifth through eighth indication is due to more first or third indications than second or fourth indications or vice versa, and whether the net count that did not cause the fifth through eighth indication indicates more first or third indications than second or fourth indications or vice versa.

18. The method defined in claim 17 wherein the making a determination comprises:

determining that the selected phase-adjacent clock signals should not be changed under the following conditions: (1) a seventh indication and the net count that did not cause the seventh indication indicates more second indications than first indications, or (2) an eighth indication and the net count that did not cause the eighth indication indicates more first indications than second indications.

19. The method defined in claim 18 further comprising:

producing a lock indication under the conditions specified in claim 18.

20. Dynamic phase alignment circuitry comprising:

circuitry for controllably selecting two phase-adjacent ones of a plurality of phase-distributed clock signals;

circuitry for comparing phases of the selected two phase-adjacent clock signals to phase of a serial data signal; and

circuitry responsive to the circuitry for comparing for controlling the circuitry for controllably selecting to change the selected phase-adjacent clock signals until the phases of the selected two phase-adjacent clock signals are predominantly on respective opposite sides of the phase of the serial data signal, and to thereafter change the selected phase-adjacent clock signals only if a first of those signals becomes more predominantly on one side of the phase of the serial data signal than a second of those signals by a predetermined amount.

21. The circuitry defined in claim 20 further comprising:

circuitry for selecting the first of the selected phase-adjacent clock signals as a basis for controlling timing of sampling of the serial data signal to recover data therefrom.

22. The circuitry defined in claim 20 wherein the circuitry for comparing comprises:

first and second phase detector circuitries for respectively comparing phases of the first and second selected phase-adjacent clock signals to the phase of the serial data signal.

23. The circuitry defined in claim 22 wherein each of the phase detector circuitries outputs a first or second signal each time that phase detector circuitry detects that the phase of the associated selected phase-adjacent clock signal is on a respective

first or second side of the phase of the serial data signal.

24. The circuitry defined in claim 23 wherein the circuitry for comparing comprises:

first and second integrator circuitries for forming net counts of the first and second signals output by the first and second phase detector circuitries, respectively.

25. The circuitry defined in claim 24 wherein the first and second integrator circuitries have respective first and second count thresholds, wherein each of the first and second integrator circuitries produces a first trigger signal when the net count of that integrator circuitry is the result of first signals greater in number than second signals by the count threshold of that integrator circuitry, and wherein each of the first and second integrator circuitries produces a second trigger signal when the net count of that integrator circuitry is the result of second signals greater in number than first signals by the count threshold of that integrator circuitry.

26. The circuitry defined in claim 25 further comprising:

circuitry for selecting the first of the selected phase-adjacent clock signals as a basis for determining timing of sampling of the serial data signal to recover data therefrom.

27. The circuitry defined in claim 26 wherein the first count threshold is greater than the second count threshold.

28. The circuitry defined in claim 27 wherein the circuitry for controlling is responsive to the first and second trigger signals of the first and second integrator circuitries.

29. The circuitry defined in claim 28 wherein the circuitry for controlling is additionally responsive to the net counts of the first and second integrator circuitries.

30. The circuitry defined in claim 29 wherein the circuitry for controlling can change the selected phase-adjacent clock signals only in response to receipt of one of the trigger signals.

31. The circuitry defined in claim 30 wherein the circuitry for controlling responds to receipt of one of the trigger signals from one of the first and second integrator circuitries by then examining the net count of the other of the first and second integrator circuitries.

32. The circuitry defined in claim 31 wherein the circuitry for controlling determines whether and how to change at least one of the selected phase-adjacent clock signals based on which of the integrator circuitries supplied the trigger signal, whether the trigger signal is a first or second trigger signal, and whether the net count of the other integrator circuitry indicates more first signals than second signals or vice versa.

33. The circuitry defined in claim 32 wherein the circuitry for controlling does not change

the selected phase-adjacent clock signals in response to receipt of a trigger signal from the second integrator circuitry under the following conditions: (1) the trigger signal from the second integrator circuitry is a first trigger signal and the net count of the first integrator circuitry indicates more second signals than first signals, or (2) the trigger signal from the second integrator circuitry is a second trigger signal and the net count of the first integrator circuitry indicates more first signals than second signals.

34. The circuitry defined in claim 33 wherein the circuitry for controlling produces a lock output signal under the conditions specified in claim 33.